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# **GE Fanuc Automation**

Programmable Control Products

Series 90<sup>™</sup>-70 System Manual for Control Software Users

GFK-1192B November 1999

# Chapter

1

# Introduction

The Series 90<sup>TM</sup>-70 PLC is a member of the GE Fanuc Series 90 PLC family of programmable logic controllers (PLCs). It is easy to install and configure, offers advanced programming features, and is designed for compatibility with other PLCs offered in the Series 90 family of PLCs. Through the use of the latest design and manufacturing technology, open architecture VME bus, and the ability to connect to Genius and FIP I/O and several CPU models, the Series 90-70 PLC provides a powerful, cost-effective platform for small applications through the very largest.

#### Software Architecture

The programming software architecture provides a platform upon which to build structured control programs. Programs may be built from many program blocks, each of which is related to a control function. Structured programs permit parallel development of a complete program as a collection of program blocks developed independently by many different individuals or OEMs. Structured programs are also easier to understand and debug. A control program may be built of many smaller program blocks, each of which can relate to a specific machine function. This approach makes it easier to isolate and associate control logic with machine functions.

The programming language and representation are based on IEC working draft 65A standard. Eventual adoption of this standard will make it easier to create programs that can be understood globally. It establishes the Series 90-70 PLC in the vanguard of the movement toward recognized international standards.

Beginning with Release 6 PLC CPUs, it has been possible to incorporate multiple programs into a folder. All of these programs can be written in C or one program can be an RLD or SFC program with the remaining programs written in C. In addition, Release 6, and later CPUs have built-in debugging capabilities for C programs and external blocks. For more information on this feature, refer to the *C Programmer's Toolkit* manual (GFK-0646C or later).

## **Terminology Used in This Manual**

The following terms are used with their defined meanings throughout this manual:

**User program**: any user-generated code, that is, an RLD program, an SFC program, or a standalone C program

**Block**: any RLD block, Parameterized Subroutine Block, or external block—an external block being either a C block or an C function block (CFBK)

#### **Fault Handling**

Faults are handled by a software alarm processor function which time-stamps and logs I/O and system faults in two tables (the PLC fault table and the I/O fault table). These tables can be displayed on the programming software screen or uploaded to a host computer or other coprocessor. Application programs can also gain access to the fault information.

#### **Hardware Configuration**

Configuration is the process of assigning physical locations, logical addresses, and parameter values to the hardware modules in the system. It may be done either before or after programming; however, it is recommended that configuration be done first.

#### **Using This Manual**

This manual is distributed with Control programming software, and describes the PLC hardware and programming features available in the CPU. Refer to the current IPI distributed with Control for CPU and programming features not described in this version of the manual.

Reference information is available in this manual, as described below:

Appendix A, *CPU Performance Data*, lists the memory size in bytes and the execution time in microseconds for each of the programming instructions. Appendix A also contains timing information for other PC tasks which, when used in conjunction with the instruction timings, can be used to predict CPU sweep times.

Appendix B, *Interpreting Faults*, describes how to interpret the message structure format when reading the PLC and I/O fault tables.

Use the worksheet in Appendix C, *Memory Allocation*, to determine the total number of bytes of user data used and how much is still available for the user program.

Refer to Appendix D, *Using Floating-Point Numbers*, for IEEE formats when dealing with floating-point math operations.

#### Revisions to This Manual

Appropriate changes have been made to this manual to reflect feature changes, corrections, and updates to existing information. The changes are:

Name of manual changed to reflect that this reference manual is for Control software users

References made to CPX and CGR model CPUs, where appropriate, throughout the manual

Bulk Memory Access information added (chapter 2)

Value for Constant Sweep timer corrected (chapter 2, pg. 2-46)

Note added after Table 2-18 regarding CPU Mode switch and description of privilege level 1 updated in table

Description of System Faults updated (chapter 3, pg. 3-2)

Appendix A, CPU Performance Data, tables revised (all information not available, will be added to a future version)

Paragraph added, beginning with "Each Ethernet Global . . . . ", page A-23 Section titled "Relative CPU Test Performance" added at end of Appendix A

# Chapter 2

# System Operation

This chapter describes certain system operations of the Series 90-70 PLC system. The table displayed below summarizes the content of each section in this chapter.

Section	Title	Description	Page
1	Basic PLC Sweep Summary	Describes the major steps in a typical PLC sweep, including application program task execution, Programmer Communications Window, System Communications Window, and Background Window.	2-2
2	User Reference Data	Describes user reference data, system status/fault references, and data types.	2-11
3	Program Organization	Describes the structure and use of LD blocks, PSB blocks, external blocks, and standalone C programs.	2-24
4	PLC Sweep Modes and Program Scheduling Modes	Explains Normal Sweep, Constant Sweep, Constant Window, Microcycle Sweep, and Stop modes. Also describes Triggered Interrupt blocks/programs and timed interrupts.	2-45
5	Run/Stop Operations	Describes the four modes of operation supported by the 90-70 PLC: Run/Outputs Enabled, Run/Outputs Disabled, Stop/IO Scan, and Stop/No IO Scan.	2-66
6	Power-Up and Power-Down Sequences	Describes the three parts of system power-up (including power-up self-test, PLC operation initialization, and system configuration), the power-down sequence, and the retention of data memory.	2-68
7	Clocks and Timers	Describes the elapsed time clock, time-of-day clock, and watchdog timers.	2-72
8	System Security	Describes protection level request from the programmer, including password assignment and block lock, OEM protection and password, and the write protect keyswitch.	2-74
9	Series 90-70 PLC I/O System	Describes I/O data mapping and diagnostic data.	2-77

# Section 1: Basic PLC Sweep Summary

The user program(s) in the Series 90-70 PLC execute in a repetitive fashion until stopped by a command from the programmer or a command from another device. In addition to executing the user program(s), the PLC obtains data from input devices, sends data to output devices, performs internal housekeeping, services the programmer, services other communications, and performs self-tests. The sequence of operations necessary to execute these components one time is called a sweep. This section summarizes the sweep phases; for more detailed information, refer to section 4 of this chapter.



# **Basic PLC Sweep**

There are seven major phases in a typical PLC sweep as shown in the following figure:

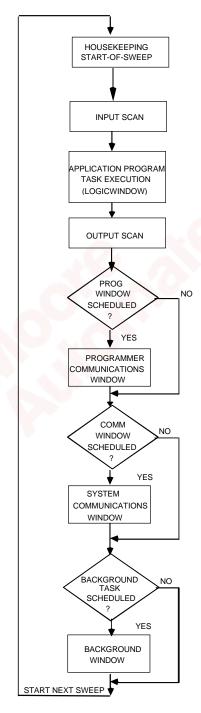


Figure 2-1. Phases of a Typical PLC Sweep

Table 2-1. Major Phases in a Typical PLC Sweep

Step	Description	
Housekeeping	Updating %S bits, determining timer update values, and determining the sweep mode occur in this phase.	
Input Scan	The CPU reads input data from Bus controllers and input modules during this phase.	
Application Program Task Execution (Logic Window)	The CPU solves the logic program(s), using data obtained from the input devices and sets bits to affect the state of output devices.	
Output Scan	The CPU writes output data to Bus controllers and output modules during this phase. The user program checksum is computed during this phase of the sweep. Polling for faulted boards also occurs during this phase.	
Programmer Communications Window	Communication with the programmer when using serial occurs here with data and/or status transfer in both directions. In addition, reconfiguration of a module or rack also occurs during this portion of the sweep.	
System Communications Window	Communications with all intelligent devices except the programmer when using a serial occur during this window. For example, supplying data to a PCM* that is driving a process display would occur during this window.	
Background Task Window	CPU self-tests occur in this window.	

<sup>\*</sup>For information about the PCM, refer to the Series 90<sup>TM</sup> Programmable Coprocessor Module and Software Support (GFK-0255).

## Housekeeping

The housekeeping portion of the sweep performs all of the tasks necessary to prepare for the start of the sweep. This includes updating %S bits, determining timer update values, and determining the mode of the sweep (Stop or Run).

# **Input Scan**

The scanning of the inputs occurs just prior to the logic solution. During the input scan, the CPU reads input data from the Genius Bus Controllers, FIP Bus Controllers, and Series 90-70 input modules.

#### Note

Beginning with Release 7.0, Ethernet global data is also read during this scan.

When referring to FIP in this scan, only periodic VCOM (MPS) services are affected. Messages are received in the System Communication Window.

Series 90-70 I/O modules are scanned from lowest to highest I/O reference address. There is no guaranteed scanning order for Bus Controllers.

#### Note

The input scan will not be performed if a program has an active Suspend I/O function on the previous sweep.

#### Application Program Task Execution (Logic Window)

The Logic Window is the phase of the sweep where user programs execute. Immediately following the completion of the input scan, the PLC Executive determines which user program(s) are to be run. Programs are then resumed and/or invoked as necessary. Solving the logic provides a new set of outputs.

Interrupt programs and blocks can execute during any phase of the sweep. Refer to section 4 for further details.

There are many ways in which program execution can be controlled to meet the system's timing requirements. The following is a partial list of the commonly used methods:

- Mask Compare and JUMP functions can be used to skip portions of the logic.
- The Suspend I/O function can be used to stop both the input scan and output scan for one sweep. I/O can be updated, as necessary, during the logic execution through the use of DO I/O instructions.
- The Service Request function can be used to suspend or change the time allotted to the window portions of the sweep.
- Program logic can be structured so that blocks and programs are called more or less frequently, depending on their importance and on timing constraints.
- Microcycle sweep mode can be used to phase programs, which need to run less often while limiting the logic window execution time.

A list of execution times for instructions can be found in Appendix A.

#### Note

In Microcycle Sweep mode, the Logic Window can be skipped or preempted as necessary by the PLC Executive.

## **Output Scan**

Outputs are scanned immediately following logic solution. During the output scan, the CPU sends output data to the Genius Bus Controllers, FIP Bus Controllers, and Series 90-70 output modules. Beginning with Release 7.0, Ethernet global data is also produced in this phase.

Series 90-70 output modules are scanned from lowest to highest I/O reference address. Bus Controllers are scanned from rack 0 to rack 7 and lowest to highest slot number within each rack.

#### Note

The output scan will not be performed if a program has an active Suspend I/O function on the current sweep.

When referring to FIP in this scan, only periodic VCOM (MPS) services are affected. Messages are received in the System Communication Window.

Polling for faulted boards also occurs during the output scan phase of the sweep. Faulted board polling recognizes replacement boards for faulted ones and reconfigures them into the system. If a board that was previously in the system or configured by the user to be in the system is listed as faulted, it must be polled periodically to determine if a new board has replaced it. Once a previously faulted board is detected as no longer faulted, reconfiguration is run in the Programmer Communications Window until the board(s) are reconfigured into the system.

The background checksum calculation also occurs during the output phase of the sweep. During each output scan phase of the sweep, the configured amount of words of user program is included in the checksum calculation. This checksum helps to ensure the integrity of the user logic while the CPU is executing. If the CPU is configured to perform a background checksum calculation (16 is the default), then this part of the output phase is performed; otherwise, it is skipped.

There are other tests performed during the Output Scan: Processor test checks basic operation of the microprocessor and BCP Opcode test checks basic operation of all BCP instructions.

#### Note

Beginning with the Release 7 CPUs, for Microcycle Sweep only, the background checksum calculation will occur during the input phase of the sweep.

#### **Programmer Communications Window**

This part of the sweep is dedicated to communicating with the programmer and performing faulted board reconfiguration. This is also when communication with the C debugger occurs. If there is a programmer attached, a debugging session is active, or if there is a board in the system that requires reconfiguration (as detected during the faulted board polling portion of the sweep), the CPU executes the Programmer Window. The Programmer Window will not execute if there is no programmer attached, no active debug session occurring, and no board to be configured in the system. During the Programmer Window, highest priority is given to board configuration. Boards are configured as needed, up to the total time allocated to the Programmer Window.

The Programmer Window is used for communication between the CPU and the two dedicated programmer ports: the built-in SNP connection and the parallel programmer connection. The CPU will complete any previously unfinished requests and then begin to process any pending requests in the queue. When the time allocated for the window expires, processing stops.

The Programmer Window time defaults to 10 milliseconds. This value can be configured and stored to the PLC or it can be changed online using your programming software.

Time and execution of the Programmer Window can also be dynamically controlled from the user program using Service Request function #3. The Programmer Communications Window time can be set to a value from 0 to 255 milliseconds.

#### Note

Even if the Programmer Window is skipped, the PLC can still respond to commands to change mode or state, or to redefine the Programmer Window if the programmer is attached through the parallel port on the Bus Transmitter Module (BTM), or by manually putting the PLC into stop mode.

### **System Communications Window**

The System Communications Window is the part of the sweep used for communication between the CPU and intelligent modules such as the PCM, Genius Bus Controller, FIP Bus Controller, and TCP/IP Ethernet modules.

At the start of the System Communications Window, the CPU will complete any previously unfinished request before executing any pending requests in the queue. When the time allocated for the window expires, processing stops.

The System Communications Window defaults to "Run to Completion" mode. This means that all currently pending requests on all intelligent option modules are processed every sweep. A different mode can be configured and stored to the PLC, or it can be changed online using your programming software.

Time and execution of the System Communications Window can also be dynamically controlled from the user program using Service Request function #4. This allows communications functions to be skipped during certain time-critical sweeps. The System Communications Window time can be set to a value from 0 to 255 milliseconds.

#### **Background Window**

A CPU self-test is performed in this window. Included in this self-test is a verification of the checksum for the 90-70 CPU operating system software.

The Background Window time defaults to 0 milliseconds. A different value can be configured and stored to the PLC, or it can be changed online using your programming software.

Time and execution of the Background Window can also be dynamically controlled from the user program using Service Request function #5. This allows background functions to be skipped during certain time-critical sweeps.

# Window Modes

The previous sections have described the phases of a typical PLC sweep. The Programmer Window, System Communications Window, and Background Window phases of the PLC sweep can be run in various modes, based on the PLC Sweep mode. (PLC sweep modes are described in detail in section 4.) The following three window modes are available:

Run-to-Completion In Run-to-Completion mode, all requests made when the window has started are serviced. When all pending requests in the given window have completed, the PLC will transition to the next phase of the sweep.

Constant

In Constant Window mode, the total amount of time that the Programmer Communications Window and Background Window run is fixed. If the time expires while in the middle of servicing a request, these windows are closed, and communications will be resumed the next sweep. If no requests are pending in this window, the PLC will cycle through these windows the specified amount of time polling for further requests. If any window is put in constant window mode, all will be in constant window mode.

#### Limited

In Limited mode, the maximum time that the window runs is fixed. If time expires while in the middle of servicing a request, the window is closed, and communications will be resumed the next time that the given window is run. If no requests are pending in this window, the PLC will proceed to the next phase of the sweep.

#### **Data Coherency in Communications Windows**

When running in Constant or Limited Window mode, the Programmer and System Communications Windows may be terminated early in all PLC sweep modes. If an external device, such as a GBC (Genius Bus Controller), is transferring a block of data, the coherency of the data block may be disrupted if the communications window is terminated prior to completing the request. The request will complete during the next sweep; however, part of the data will have resulted from one sweep and the remainder will be from the following sweep. When the PLC is in Normal Sweep mode and the Communications Window is in Run-to-Completion mode, the data coherency problem described above does not exist.



# **CPU Sweep in STOP Mode**

The 90-70 PLC has two modes of operation while it is in Stop mode: Stop/NoIO and Stop/IOScan  $\mbox{.}$ 

When the PLC is in Stop/NoIO mode the Input Scan, Logic Window, and Output Scan phases of the PLC sweep are skipped.

When the PLC is in Stop/IOScan mode the Logic Window phase of the PLC is skipped but the Input Scan and Output Scan phases are performed each sweep.

In both Stop/NoIO and Stop/IOScan modes, the two Communications Windows run in Run-to-Completion mode and the Background Window runs in Limited mode with a 10 millisecond limit.

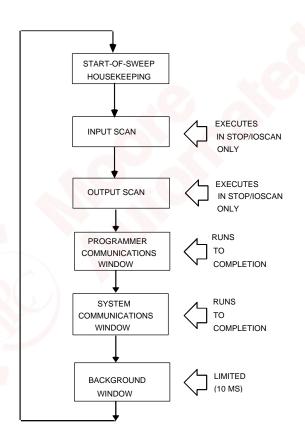


Figure 2-2. CPU Sweep in Stop/NoIO and Stop/IOScan Mode

Note

Stop/IOScan is not supported in Microcycle Sweep mode.

#### **PLC Sweep Modes**

The 90-70 PLC supports four PLC sweep modes:

#### **Normal Sweep**

In Normal Sweep mode, each PLC sweep can consume a variable amount of time. The Logic Window is executed in its entirety each sweep. The Communications and Background Windows can be set to execute in a Limited or Run-to-Completion mode.

#### Constant Sweep

In Constant Sweep mode, each PLC sweep begins at a user-specified Constant Sweep time after the previous PLC sweep began. The Logic Window is executed in its entirety each sweep. If there is sufficient time at the end of the sweep, the PLC will alternate among the Communications and Background Windows, allowing them to execute until it is time for the next sweep to begin.

#### Constant Window

In Constant Window mode, each PLC sweep can consume a variable amount of time. The Logic Window is executed in its entirety each sweep. The PLC will alternate among the Communications and Background Windows, allowing them to execute for a time equal to the user-specified Constant Window timer.

#### Microcycle Sweep

In Microcycle Sweep mode, like Constant Sweep mode, each PLC sweep takes a fixed amount of time. The user specifies the total sweep time (base cycle time) and the total time for the Communications and Background Windows. The Logic Window can be preempted in order to maintain the total sweep time and the Communications Windows and Background Window times. To satisfy the specified window times, the PLC alternates among the Programmer Communications Window, the System Communications Window, and the Background Window, allowing them to execute until it is time for the next sweep to begin.

#### **Note**

The information presented above summarizes the different sweep modes. For detailed information on PLC Sweep Modes, refer to "PLC Sweep Modes and Program Scheduling Modes" in section 4 of this chapter.

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