

Trusted TMR Processor Interface Adapter (T8120, T8121, T8122, T8123)

Product Overview

This document provides general information for the Trusted® Processor Interface Adapter T812X. The Adapter provides easy access to the communications ports of the Trusted Triple Modular Redundant (TMR) Processor (T8110B & T8111) in the Controller Chassis for the Distributed Control System (DCS) and other links. The unit is also used to enable a number of extended facilities available on the Trusted TMR Processor including facilities for the reception of IRIG-B time synchronisation signals, enabling the use of Dual ('enhanced') Peer to Peer and enabling the Trusted System to become MODBUS Master.

Features:

- Allows easy access for external systems to communicate with a Trusted TMR Processor.
- Easy installation (connects directly to the rear of the Controller Chassis).
- Two RS422/485 configurable 2 or 4 wire connections.
- One RS422/485 2 wire connection.
- Fault/fail connections for Active and Standby Processors.
- Processor diagnostics connection.
- PSU shutdown monitor connections.
- Option for connecting IRIG-B122 and IRIG-B002 time synchronisation signals.
- Option to enable MODBUS Master on the Trusted Communications Interface.

ISSUE RECORD

Issue	Date	Comments
6	Sep 05	Format
7	Aug 06	Dual Peer to Peer
8	Sep 07	Port purposes
9	Sep 14	Fault/Fail connector identity
10	Sep 15	Rebranded and reformatted with standardisation of the Relative Humidity Range and Operating Temperature specifications
11	Apr 16	Updated to incorporate IEEE standards and correct typographical errors
12	Oct 19	Updated Figure 2 Adapter Layout Updated Table 2 Connector SK1 Pinout Updated Section 1.2 Fault/Fail Connectors Removed Diagnostic Connector (J4) information Split J5 into two connectors, J5 and J13 Updated Table 7 Mating Connectors Added Table 8 Single Point Connection Added Table 9 Multi-drop Connection Updated Section 3.2 IRIG-B Ports Updated Specifications table

Table of Contents

1.	Description	3
1.1.	Processor Interface Connector (SK1)	5
1.2.	Fault/Fail Connectors (J2 and J3) (J17 and J15)	6
1.3.	PSU Shutdown Monitor Connector (J6)	6
1.4.	Serial Port 1 (Diagnostic) Connectors (J7 and J12).....	6
1.5.	Serial Ports 2 and 3 Connectors (J8 to J11)	7
1.6.	IRIG B Connectors (J5 and J13).....	7
1.7.	Mating Connectors.....	8
2.	Installation	9
3.	Input Configuration.....	11
3.1.	Serial Ports	11
3.2.	IRIG-B Ports	12
4.	Available Operations	13
5.	Specifications.....	15

1. Description

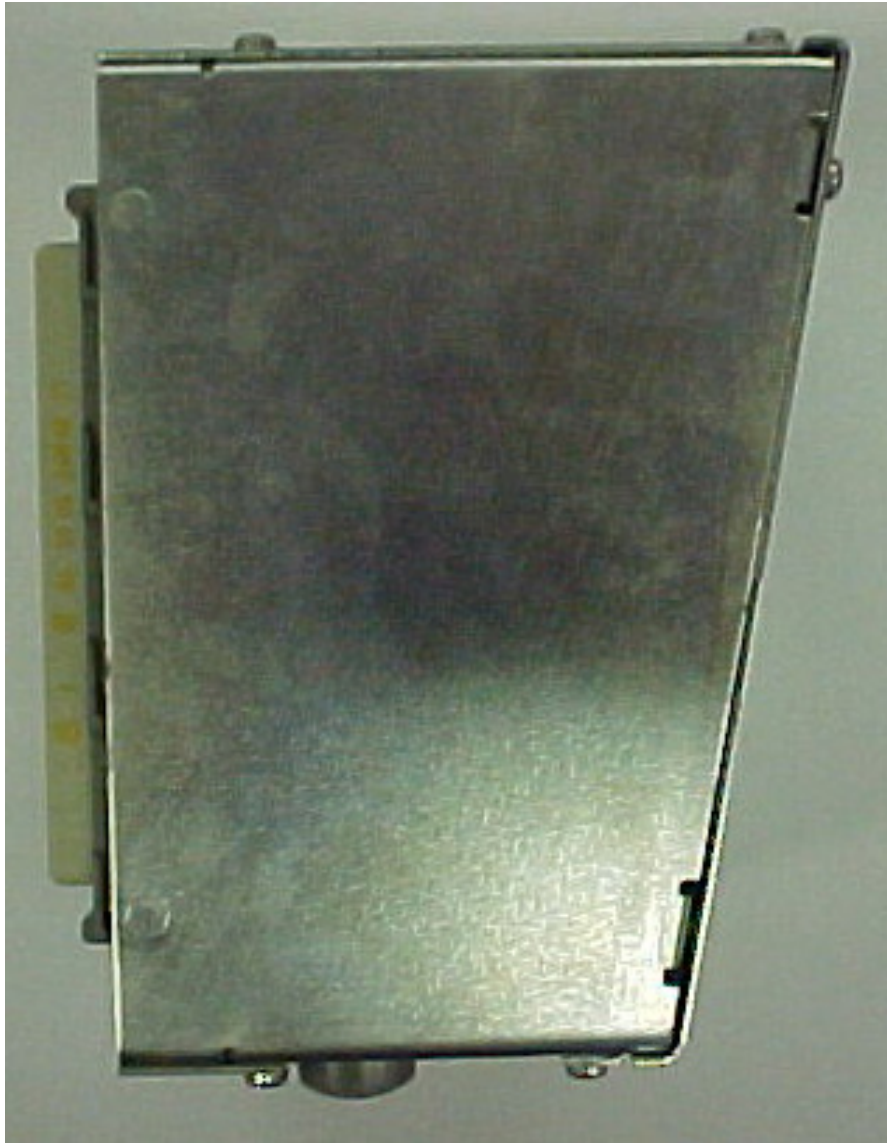


Figure 1 Photo T812X

The Trusted Processor Interface Adapter T812x is designed to be connected directly to the rear of a Trusted TMR Processor position in a Trusted Controller Chassis T8100. The Adapter provides a communications connection interface between the Trusted TMR Processor and remote systems. The Adapter also provides the option of connecting IRIG-B time synchronisation signals to the Processor. Connection between the Adapter and the Trusted TMR Processor is via two 48-way DIN41612 E-type connectors (SK1), one each for connection to the Active and Standby Processors.

Figure 2 shows the physical layout of serial port, diagnostics and IRIG-B connectors on the Adapter printed circuit board (PCB).

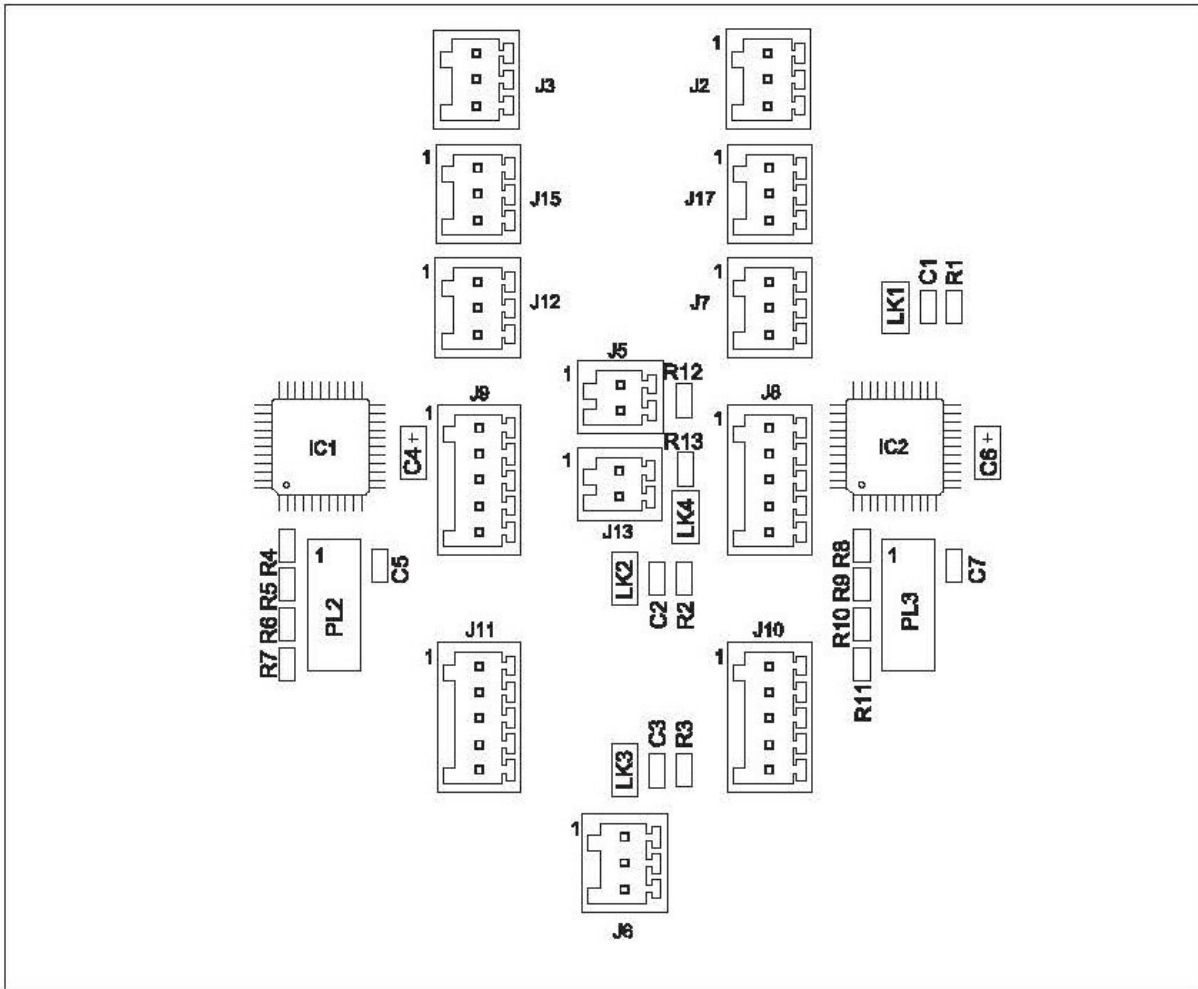


Figure 2 Adapter Layout

The Adapter comprises a PCB on which the communications ports, IRIG-B connectors and both SK1 sockets (connectors to the Active/Standby Trusted TMR Processors) are mounted. The Adapter is contained within a metal enclosure and is designed to be clipped onto the appropriate connector at the rear of the Controller Chassis. Release buttons are provided to enable the Adapter to be disconnected.

The communication ports available at the Adapter are RS422/RS485 2 wire on Port 1, and RS422/RS485 2 or 4 wire on Ports 2 and 3.

An earth point is provided on the PCB so that the Chassis earth of the Processor will be connected to the shell of the Adapter and module rack earth. It is an important safety and Electrostatic Discharge (ESD) requirement that the equipotential bonding is connected and maintained.

1.1. Processor Interface Connector (SK1)

SK1 is a 48-way DIN41612, E-type connector.

Pin	CONNECTOR SK1 PINOUT		
	A	C	E
2	Fault Relay (NC)	DIAG_RTN (NC)	Failed Relay (NC)
4	Fault Relay (Common)	DIAG_IN_1 (NC)	Failed Relay (Common)
6	Fault Relay (NO)	0 V Port 1	Failed Relay (NO)
8	N.C.	Serial Port 1 B	N.C.
10	5 V_D	Serial Port 1 A	IRIG B122+
12	DATA_OUT	0 V Port 2	IRIG B122-
14	ENABLE	Serial Port 2 B TX	Reserved
16	DATA_IN	Serial Port 2 A TX	Reserved
18	CLK	Serial Port 2 B RX/TX	IRIG-B002-
20	0 V	Serial Port 2 A RX/TX	IRIG-B002+
22	Chassis GND	0 V Port 3	Chassis GND
24	Chassis GND	Serial Port 3 B TX	Chassis GND
26	Chassis GND	Serial Port 3 A TX	Chassis GND
28	24 V PSU 1 LV Warning	Serial Port 3 B RX/TX	24 V PSU 1 Shutdown
30	24 V PSU 2 LV Warning	Serial Port 3 A RX/TX	24 V PSU 2 Shutdown
32	24 V Return	24 V Return	24 V Return

Table 1 Connector SK1 Pinout

1.2. Fault/Fail Connectors (J2 and J3) (J17 and J15)

J2, J3, J15 and J17 are Phoenix contact 2.5 mm pitch connectors.

Pin	Service
1.	FAULT_n_NC
2.	FAULT_n_COM
3.	FAULT_n_NO

Pin	Service
1.	FAIL_n_NC
2.	FAIL_n_COM
3.	FAIL_n_NO

Table 2 Fault/Fail Connectors

Note: n=1 for connectors J2 and J17, n=2 for connectors J3 and J15 providing fault and fail connections for the Active and Standby Processors respectively. FAULT NC relay contacts open on any system fault which sets the Processor System Healthy LED flashing red. FAIL NC relay contacts open on Processor shutdown.

1.3. PSU Shutdown Monitor Connector (J6)

J6 is Phoenix contact 2.5 mm pitch connector. These two system inputs are made available to the application on the Processor's complex I/O equipment definition. The inputs expect volt-free contacts to the RTN pin.

Pin	Service
1	24 V_PSU1_SHUTDOWN
2	24 V_PSU2_SHUTDOWN
3	24 V_RTN

Table 3 PSU S/D Monitor Connection

1.4. Serial Port 1 (Diagnostic) Connectors (J7 and J12)

J7 and J12 are Phoenix 2.5 mm pitch connectors.

Pin	Service
1	0 V
2	SERIAL_1_B
3	SERIAL_1_A

Table 4 Serial Port 1 Diagnostic Connectors

1.5. Serial Ports 2 and 3 Connectors (J8 to J11)

These are Phoenix 2.5 mm pitch connectors.

Pin	Service
1	0 V
2	SERIAL_TX_B
3	SERIAL_TX_A
4	SERIAL_RX/TX_B
5	SERIAL_RX/TX_A

Table 5 Serial Ports 2 and 3 Connectors

1.6. IRIG B Connectors (J5 and J13)

J5 and J13 Phoenix 2.5 mm pitch connectors.

J5

Pin	Service
1	IRIG-B122+
2	IRIG-B122-

J13

Pin	Service
1	IRIG-B002-
2	IRIG-B002+

Table 6 IRIG-B Connectors

1.7. Mating Connectors

The following table lists the connectors required to mate with the Trusted Processor Interface Adapter.

Connector	Phoenix Contact Part No	ICS Part No	No of Ways
J5, J13	18 81 32 5	3JX073	2
J2, J3, J6,J7,J12, J15, J17	18 81 33 8	3JX075	3
J8,J9,J10,J11	18 81 35 4	3JX076	5

Table 7 Mating Connectors

2. Installation

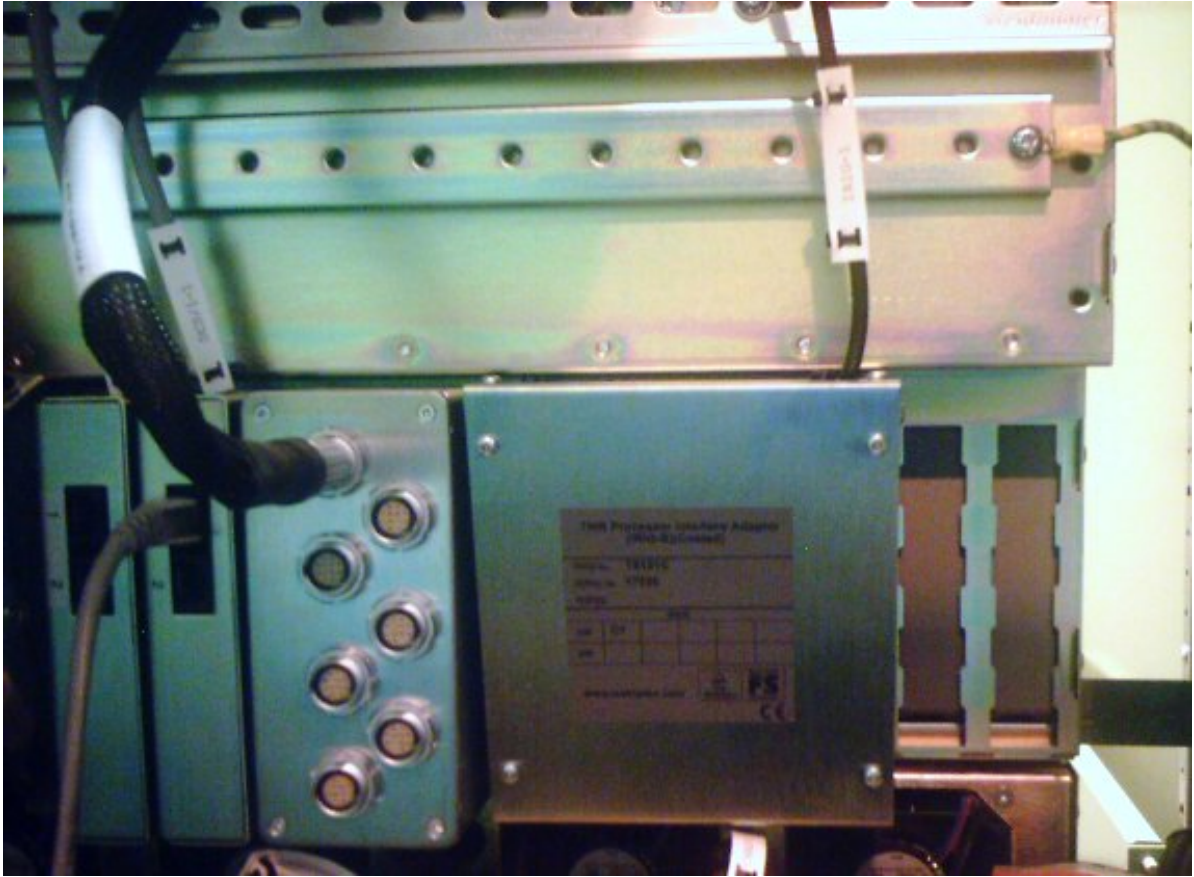


Figure 3 Correct Installation Position

The Adapter should be fitted on the rear of the chassis behind the Processor slots, as shown above. The two connectors should fit into the third and sixth slots from the right, where the Processor connectors will fit. In the correct position, two empty slots will be visible on the right. Insert the Adapter into position about 5 mm lower than its final position, and ensure it is slotted in on both sides. Raise the Adapter upwards until the retaining clips click into place.

Page intentionally left blank

3. Input Configuration

3.1. Serial Ports

The serial ports connectors are arranged so that multi-drop RS422/485 connections can be easily configured. J7, J8 and J10 together with LK1, LK2 and LK3 form the basic terminations for ports 1, 2 and 3 respectively.

Port No.	Serial In	Termination
Port 1	J7	Fit LK1
Port 2	J8	Fit LK2
Port 3	J10	Fit LK3

Table 8 Single Point Connection

Port No.	Serial In	Serial Out
Port 1	J7	J12
Port 2	J8	J9
Port 3	J10	J11

Table 9 Multi-drop Connection

For a single point connection the termination would be made to the relevant connector and its corresponding link would be fitted. For a multi-drop connection the 'incoming' connections would be made to the connections listed above and the 'outgoing' to J12, J9 or J11 for ports 1 to 3 respectively. This time however, the link will be removed as only the last connection on a multi-drop chain should be terminated.

The provision of the two connectors for each serial port will enable quicker configuration of serial cabling as there is now no need to terminate two cables onto the same connector. The links LK1 to LK3 provide the serial ports with an easy way to add 120 Ω AC termination onto the receivers extremely close to the receiving devices.

The 4 wire serial ports 2 and 3 have connectors that are pin compatible with those used on the Trusted Communications Interface Termination Unit (T8153).

Serial connections should use screened twisted pair cable with the A-B signals connected as a pair. The screen should be connected to chassis ground at one end only. Some equipment may require a common 0 V connection. In order to operate correctly, the 0 V on the connector should be connected to 0 V on the other equipment to facilitate this.

Note: RS485 bus biasing is implemented differently in the T8111 compared to legacy T8110. For more information and technical support, refer to the Rockwell Automation Support Centre:

<http://rockwellautomation.custhelp.com>

Further information on serial port configuration can be found in the standards listed below:

- EIA/TIA-422-B
- EIA-485
- CCITT V.11

3.2. IRIG-B Ports

The IRIG-B002 input is a pulse width modulated signal at 100bits/s and uses RS422 voltage levels. Connection to this port should be by twisted pair cable. A 120 Ω termination (R13) is provided on the module. The termination resistance connects to the circuit by fitting LK4. For multi-drop configurations, remove LK4 from all but the last interface adapter.

The IRIG-B122 input is a 1 kHz amplitude modulated signal where the modulating signal has the same format as IRIG-B002. The peak amplitude (mark) of the input signal is nominally 1 V to 6 V into 600 Ω . The Trusted TMR Processor is able to receive signals in the range 0.25 V PK-PK to 10 V PK-PK. IRIG-B122 is normally provide via co-axial cable although any suitable medium would be acceptable.

Further information on IRIG configuration can be found in the standards listed below:

- Range Commanders Council IRIG STANDARD 200-98
- IEEE Std 1344-1995 Annex F.2

4. Available Operations

The following table lists the variants of the Trusted Processor Adapter Unit and the Trusted TMR Processor options that can be made available by using them. All the variants below will enable the use of Dual ('enhanced') Peer to Peer with other Trusted Systems, using the dxpnc40 I/O definition and its associated data transfer I/O definitions.

Variant	Options Enabled
T8120	None. Basic module with terminations for serial ports and ancillary connections.
T8121	IRIG-B. Enables decode of IRIG-B002 or IRIG-B122 time synchronisation signals by the Trusted TMR Processor.
T8122	MODBUS Master. Enables the Trusted System to operate as MODBUS Master. See Note.
T8123	IRIG-B and MODBUS Master. Enables IRIG-B time signal decode and MODBUS Master operation.

Table 10 Available Options

Note: The Trusted Communications Interface (T815X) is also required for MODBUS Master operation. The serial ports on the Trusted TMR Processor can only be used for MODBUS Slave operation.

Page intentionally left blank

5. Specifications

Power Supply	Powered from Trusted TMR Processor
Power Dissipation	0.1 W
Isolation Between; Rear Serial Ports, IRIG Ports, Relay Ports and Chassis	50 V Reinforced (continuous) ⁽¹⁾ 250 V Basic (fault) ⁽²⁾ [Type tested at 2436 Vdc for 60 s]
Fusing	None
Ports Port 1 Ports 2 and 3 IRIG B	RS422/485 RS422/485 IRIG-B122 and IRIG-B002 on a single connector
Operating Temperature	0 °C to +60 °C (+32 °F to +140 °F)
Storage Temperature	-25 °C to +70 °C (-13 °F to +158 °F)
Relative Humidity – Operating and Storage	10 % – 95 %, non-condensing
Environmental Specifications	Refer to Trusted 8000 - Series B: International Safety & Environmental Approvals, publication ICSTT-TD003
Dimensions Height: Width: Depth:	138 mm (5.43 in) 120 mm (4.72 in) 108 mm (4.25 in)
Weight	877 g (1.93 lb)

Note 1) 50 Vrms Secondary circuit derived from Mains, OVC II up to 300V.

Note 2) 250 Vrms Mains circuit, OVC II up to 300V. Exposure to voltages at these levels shall be temporally constrained consistent with the system MTTR.